REMARKS

Claim 5 has been amended. No new claims have been added. Claims 39 and 57-60 have been previously canceled. Claims 1-56 are pending.

Claim 5 stands objected to due to a minor informality. Claim 5 has been amended as suggested in the Office Action. Accordingly, the objection to claim 5 should be withdrawn.

Claims 1-2, 16-20, 34-35, 38, 40, 51-52, and 55-56 stand rejected under 35 U.S.C. 102(e) as being anticipated by Ajanovic (U.S. Patent No. 6,516,375).

Claims 3-5, 21-33, 36-37, and 41-50 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic in view of Frame (U.S. Patent No. 5,349,690).

Claims 53 and 54 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic in view of Singh (U.S. Patent No. 6,609,171).

Claim 1 recites, inter alia, "A bus arbitration method for ... system ... comprising a link bus, said link bus comprising a link bus hub and a plurality of link bus segments each link bus segment comprising a plurality of lines for communicating commands, addresses, data, and a single-bit link status signal, each link bus segment coupled to said link bus hub and one respective satellite device to form a point-to-point link between said link bus hub and respective satellite device, one of said respective satellite device being a first device, a processor coupled to said hub device via a processor bus, and a memory device coupled to said link bus hub by a memory bus, said method comprising the steps of: issuing, from one of the first device and the hub device, an arbitration request on a portion of said plurality of lines associated with said single-bit link status signal of the link bus."

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Claim 19 recites, inter alia, "A method of arbitrating control of a link bus of a computer system, the link bus comprising a link bus hub and a plurality of link bus segments, each link bus segment comprising a plurality of lines for communicating commands, addresses, data, and a single-bit link status signal, each link bus segment coupled to said link bus hub and one respective satellite device to form a point-to-point link between said link bus hub and respective satellite device, said hub device coupled to a processor of said computer system by a processor bus and coupled to a memory device of said computer system by a memory bus, the link bus being a source strobed bus, said method comprising the steps of: time-multiplexing, from one of the satellite device and the hub device, an arbitration request signal on the single-bit link status line."

Claim 34 recites, inter alia, "A ... system comprising: ... a link bus ... comprising a link bus hub and a plurality of link bus segments, each link bus segment comprising a plurality of lines for communicating commands, addresses, data, and a single-bit link status signal, each link bus segment coupled to said link bus hub and one respective satellite device to form a point-to-point link between said link bus hub and respective satellite device, one of said respective satellite device being a first device, said link bus hub being coupled to said processor via a processor bus; wherein said first device and said link hub arbitrate a control of said link bus by issuing, from one of said satellite device and said link hub, an arbitration request on a portion of said plurality of lines associated with said single-bit link status signal of the link bus."

Claim 51 recites, inter alia, "A ... system comprising: a processor; a link bus, said link bus comprising a link bus hub and a plurality of link bus segments, each link bus segment comprising a plurality of lines for communicating commands, addresses, data, and a single-bit link status signal, each link bus segment coupled to said link bus hub and one respective satellite device to form a point-to-point link between said link

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bus hub and respective satellite device, one of said respective satellite device being a first device, said link bus hub being coupled to said processor via a first bus; wherein said first device multiplexes an arbitration signal on a portion of said lines associated with said single-bit link bus status signal ... to become a master of said link bus during transmissions to said link hub, and said link bus hub multiplexes another arbitration signal on said portion of said lines associated with said single-bit link bus status signal ... to become a master of said link bus during transmissions to said first device."

Ajanovic discloses a method and apparatus for a PC utilizing a hub based interface to emulate a PCI-bus based interface.

Claims 1, 19, 34, and 51 additionally recite that each link bus segment comprises "a plurality of lines for communicating commands, addresses, and data, and a single-bit link status signal," and that the method includes the step of "issuing ... an arbitration request on a portion of said plurality of lines associated with said single-bit link status signal of the link bus" (claims 1 and 34) or "time-multiplexing, from one of the satellite device and the hub device, an arbitration request signal on the single-bit link status line" (claim 19), or "said first device multiplexes an arbitration signal on a portion of said lines associated with said single-bit link bus status signal ... to become a master of said link bus during transmissions to said link hub, and said link bus hub multiplexes another arbitration signal on said portion of said lines associated with said single-bit link bus status signal ... to become a master of said link bus during transmissions to said first device" (claim 51).

Ajanovic fails to disclose or suggest a "each link bus segment comprising ... a single-bit link status signal." Ajanovic in fact teaches to the contrary and discloses using two independent status signals, namely RQA and RQB. As Ajanovic teaches a "hub interface 1400 comprises ... an additional differential pair of source synchronous

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strobe signals..." and two unidireclty arbitration request signals. Column 10, lines 25 –

35. With respect to any two devices in Ajanovic's system, (e.g., a hug agent and a hub),

one device is known as device A and the other device is known as device B. Each

device has its own outgoing arbitration request line (i.e., RQA for device A and RQB for

device B) for requesting an arbitration request. Column 10, line 5 – column 12, line 30;

See Table 3 (columns 10-11); See Fig. 11. Since RQA and RQB are independent signals

they cannot correspond to the claimed "single-bit link status signal" because the

combination of these two independent signals RQA, RQB encode 2 bits of information.

Ajanovic is required to utilize multiple arbitration signal lines because Ajanovic awards

arbitration to the first device which requests the bus, thereby requiring a multi-bit

status information, as a single bit signal cannot differentiate between the four possible

states which arise when two devices are competing in a race (i.e., devices A and B both

do not request arbitration, device A requests arbitration first, device B request

arbitration first, devices A and B request arbitration simultaneously). See Column 8,

lines 48-49.

Accordingly, Ajanovic cannot be fairly stated to disclose or suggest the

subject matter recited in independent claims 1, 19, 34, and 51.

The Office Action further cites to Frame and Rosen. Each of these references,

however, fail to supply any teaching or suggestion, which when taken individually or

in combination, discloses or suggest the claimed invention. More specifically:

Frame discloses a bus system in which individual bus devices are assigned a

fixed priority and the highest priority device wins arbitration. Column 2, line 29-31 and

49-51. However, Frame does not even disclose a hub based bus system, and therefore

cannot disclose or suggest the recited "link bus." Frame further does not disclose the

use of the claimed "single-bit link status signal."

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Singh discloses a conventional multi-drop bus system which supports a quad pumped bus architecture and protocol. Referring to Fig. 1, it can be seen that Singh's computer system 100 utilizes a conventional non-hub based system interface 116, utilizing multiple I/O interfaces 118, controllers 120, and bridges 124 to facilitate communication between various devices and the processors 110, 112, 114.

Thus, none of the additional references (i.e., Frame and Singh), whether taken individually, or in combination, discloses or suggest the above quoted limitations of independent claims 1, 19, 34, and 51.

Independent claims 1, 19, 34, and 51 are believed to be allowable over the prior art of record. The depending claims, i.e., claims 2-18, 20-33, 35-38, 40-50, 52-56 are also believed to be allowable for at least the same reason as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: June 6, 2005   Respectfully submitted,

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